ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device including a semiconductor substrate1, a plurality of memory cells 1a on the semiconductor substrate including transistors having floating gate electrodes and control gate electrodes. Source lines 30 are formed in a self-alignment manner with respect to a control gate electrodes. The surface of the semiconductor substrate 1 has such a periodical unevenness along the source lines 30 which has a diffusion layer 30a that an impurity is distributed along the surface of the semiconductor substrate 1 and a buried diffusion layer 30b that an impurity is distributed at a position deeper than said diffusion layer 30a.   The buried diffusion layer 30b connects a plurality of portions of the diffusion layers 30a under the bottom surface 5b of the recess portion 5 to each other.